UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/782,697	02/18/2004	Bulent M. Basol	NVLUS.031CP1	5582

20995 7590 07/06/2007

KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

EXAMINER	
TRINH, MICHAEL MANH	

ART UNIT	PAPER NUMBER
2822	

NOTIFICATION DATE	DELIVERY MODE
07/06/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

jcartee@kmob.com
eOAPilot@kmob.com

Office Action Summary	Application No.	Applicant(s)	
	10/782,697	BASOL ET AL.	
	Examiner	Art Unit	
	Michael Trinh	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10,16-21,25 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,16-21,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

*** This office action is in response to Applicant's Amendment filed April 19, 2007. Claims 1-10,16-21,25-26 are pending, in which claims 25-26 have been newly added. Claims 11-15 and 22-24 were cancelled by Applicant.

*** The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Objections

1. Claims 25-26 are objected as being unclear for what is "removing", since there are two "removing" in claims 1+2, and claims 16+17. Appropriate correction is respectfully requested.

Claim Rejections - 35 USC § 103

2. Claims 1-5,7-9,16-19,21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Collins (2004/0038052) and Nogami (2001/0041447).

Re claim 1, Hongo teaches (at Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45) a method of forming a layer of a conductive material on a wafer, wherein a seed layer coats a front surface and an edge surface of the wafer, and wherein the edge surface includes a back edge surface, a bevel surface and a front edge surface, the method comprising the steps of: removing the seed layer 83 from the back edge surface and the bevel surface; and forming the conductive material 85 onto the seed layer 83 coating the front edge surface and the front surface of the wafer (Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45). Re claim 16, Hongo teaches (at Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45) a method of forming a layer of a conductive material 85 on a wafer comprising a front surface, a back surface and an edge surface, the edge surface including a back edge surface, a bevel surface and a front edge surface, the method comprising the steps of: depositing a seed layer 83 on the front surface and the edge surface of the wafer; removing the seed layer 83 from the back edge surface and the bevel surface; and forming the layer by depositing the conductive material 85 onto the seed layer coating the front edge surface and the front surface (Figs 8,7; col 4, lines 50-57; Figs 2,1; col 1, lines 19-45). Re claims 2,17, wherein, as shown in Figs 8,7, removing at least a part of the layer 83 which is on the front edge surface. Re claims 3,18, wherein the wafer is rotated during the

step of removing the seed layer 83 (Figs 3,7-8; col 2, line 63 through col 4). Re claims 4,19, applying a process solution is applied onto the back edge surface of the wafer while it is rotated (Fig 3; col 3, line 3 through col 4). Re claims 5,21, wherein the step of removing comprises chemical etching (Figs 7-8,3; col 4, lines 50 through col 5, line 12; col 3, line 45 through col 4). Re claim 7, the wafer is rotated prior to the step of removing the at least a part of the layer 83 (Figs 3,7-8; col 3, lines 3-45; col 2, line 63 through col 4). Re claim 8, wherein a process solution is applied to the at least a part of the layer while the wafer is rotated (Figs 3,7,8; col 3, line 3 through col 4, line 67). Re claim 9, wherein the step of removing the at least a part of the layer comprises chemical etching (Figs 7-8,3; col 4, lines 50 through col 5, line 12; col 3, line 45 through col 4).

Hongo teaches forming the conductive material 85 onto the seed layer 83 before removing the seed layer 83 from the back edge surface and the bevel surface, while claim 1 recites forming the conductive material after removing the seed layer from the back edge surface and the bevel surface.

However, Collins teaches (at Figs 2B-2C,3; paragraphs 21-28,11-13) forming the conductive material after removing of the seed layer 120 (Fig 2B) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed layer 120 (Fig 2C) on the front surface of the wafer (Fig 2C). Nogami teaches (at Figs (2A-2C) forming a conductive material on the seed/barrier layer 116,114 after removing of the barrier/seed layer (Figs 2A-2C; paragraphs 17-21) from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed/barrier layer on the front surface of the wafer (Fig 2C)

Therefore, the subject matter as a whole would have been obvious to one of ordinary skill in the art at the time the invention was made to forming the conductive material on the seed layer of Hongo after removing the seed layer from the edge surface including the bevel surface, the back edge surface, and part of the front edge surface so as to leave the seed layer on the front surface of the wafer, as taught by Collins and Nogami. This is because of the desirability to prevent forming the conductive material at unwanted edge surface, and because of the desirability to deposit the conductive material at a selected portion on the seed layer at the front surface of the wafer so that the step of removing the conductive material at the edge surfaces

after depositing the conductive material is not necessarily needed, thereby reducing processing steps. This is also because of the desirability to provide copper interconnects with reduced contamination due to copper deposited at the edge or rear of the substrate (Nogami, paragraphs 21,20).

3. Claims 6,10,20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Collins (2004/0038052) and Nogami (2001/0041447), as applied to claims 1-5,7-9,16-19,21 above, and further of Volodarsky et al (6,352,623).

Hongo, Collins and Nogami teach a method for forming a conductive layer as applied to claims 1-5,7-9,16-19,21 above.

The references including Hongo already teaches removing the layer by chemical etching while claims 6,10 and 20 recite removing the layer by electrochemical etching.

However, Volodarsky teaches (at Figs 1-2; col 5, lines 8-27) employing an ECMD process and apparatus for depositing and removing a layer by electrochemical etching or chemical etching.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the layer of Hongo by employing the ECMD process for removing a layer by electrochemical etching or chemical etching as taught by Volodarsky. This is because electrochemical etching and chemical etching are alternative and art recognized equivalent etching process for removing a portion of the layer from the wafer, wherein the electrochemical etching is an effective process for removing a layer in a reliable manner.

4. Claims 25,26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hongo et al (6,615,854) taken with Collins (2004/0038052) and Nogami (2001/0041447), as applied to claims 1-5,7-9,16-19,21 above, and further of Ulrich et al (5,897,379).

Hongo, Collins and Nogami teach a method for forming a conductive layer as applied to claims 1-5,7-9,16-19,21 above.

Claims 25-26 recite that the step of removing is after forming the conductive material layer.

However, Hongo teaches (at Figs 7-8; col 4, line 50 through col 6) removing a portion of the conductive material 85 layer after forming the conductive material layer 85. Ulrich also teaches (at Figs 3-5; col 5, line 56 through col 6; Figs 9-11; col 7, lines 22-50) removing a portion of the conductive material 32 layer after forming the conductive material layer 32.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to continue the semiconductor fabrication of the references including Hongo by removing a portion of the conductive material layer after forming the conductive material layer, as taught by Ulrich and Hongo. This is because of the desirability to remove the unwanted conductive material layer from the perimeter of the wafer, and because of the desirability to pattern the conductive material layer in order to form an electrical interconnection for an semiconductor device.

Response to Amendment

5. Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

****

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

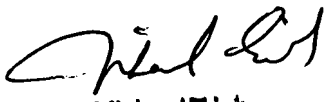
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

****

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael M. Trinh whose telephone number is (571) 272-1847. The examiner can normally be reached on M-F: 9:00 Am to 5:30 Pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The central fax phone number is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).
Oacs-24-1



Michael Trinh
Primary Examiner